CLAIMS

We claim:

1. A method for processing a data signal, comprising:

transmitting the data signal through an electrical backplane; and

receiving the data signal after being transmitted through the electrical backplane, wherein the received data signal is interpreted as a duobinary data signal.

2. The invention of claim 1, further comprising precoding a binary data signal, wherein the data signal transmitted through the electrical backplane is based on the precoded binary data signal.

3. The invention of claim 1, further comprising filtering the data signal prior to interpreting the data signal as the duobinary data signal.

4. The invention of claim 3, wherein the filtering is implemented before transmission through the electrical backplane.

5. The invention of claim 3, wherein the filtering comprises equalizing filtering.

6. The invention of claim 3, wherein the filtering is designed to emphasize high-frequency components in the data signal and flatten group delay of the electrical backplane.

7. The invention of claim 3, wherein the filtering is implemented using an FIR filter.

8. The invention of claim 3, wherein the filtering:

delays a first copy of the data signal;

attenuates the delayed first copy; and

adds the delayed first copy to a second copy of the data signal to generate the filtered data signal.

9. The invention of claim 3, wherein the combination of the filtering and the transmission through the electrical backplane approximates binary-to-duobinary conversion.

10. The invention of claim 1, wherein duobinary-to-binary (D/B) conversion is applied to the received data signal to generate a binary data signal.

11. The invention of claim 10, wherein the D/B conversion comprises:

comparing amplitude of the received data signal with first and second threshold voltages to generate first and second binary streams; and

applying a logic function to the first and second binary streams to generate the binary data signal.

12. The invention of claim 11, wherein the logic function comprises an exclusive-OR (XOR) function.

13. The invention of claim 11, wherein the logic function comprises an exclusive-NOR (XNOR) function.

14. The invention of claim 11, wherein:

the data signal is an NRZ binary data signal; and

the first and second threshold voltages are selected such that one of the first and second binary streams is always zero or always one.

15. The invention of claim 1, wherein the electrical backplane comprises a multi-layer board.

16. The invention of claim 1, further comprising:

precoding a binary data signal, wherein the data signal transmitted through the electrical backplane is based on the precoded binary data signal;

filtering the data signal prior to interpreting the data signal as the duobinary data signal; and

applying duobinary-to-binary conversion to the received data signal to generate a binary data signal.

17. The invention of claim 16, wherein:

the combination of the filtering and the transmission through the electrical backplane approximates binary-to-duobinary conversion; and

the duobinary-to-binary conversion comprises:

comparing amplitude of the received data signal with first and second threshold voltages to generate first and second binary streams; and

applying a logic function to the first and second binary streams to generate the binary data signal.

18. A transmission system for a data signal, comprising:

a transmitter subsystem adapted to transmit the data signal though an electrical backplane; and

a receiver subsystem adapted to receive the data signal after being transmitted through the electrical backplane, wherein the received data signal is interpreted as a duobinary data signal.

19. The invention of claim 18, further comprising a filter adapted to filter the data signal prior to the data signal being interpreted as the duobinary data signal.

20. The invention of claim 19, wherein the filter is designed to emphasize high-frequency components in the data signal and flatten group delay of the electrical backplane.

21. The invention of claim 19, wherein the filter comprises:

one or more delays adapted to delay a first copy of the data signal;

an attenuator adapted to attenuate the delayed first copy; and

a summing node adapted to add the attenuated, delayed first copy to a second copy of the data signal to generate the filtered data signal.

22. The invention of claim 21, wherein the filter further comprises a selector connected to receive an output from each of a plurality of delays and adapted to select one of the delay outputs as the signal applied to the attenuator.

23. The invention of claim 19, wherein the combination of the filter and the electrical backplane approximates a binary-to-duobinary converter.

24. The invention of claim 18, wherein the receiver subsystem comprises a duobinary-to-binary (D/B) converter adapted to apply duobinary-to-binary conversion to the received data signal to generate a binary data signal.

25. The invention of claim 24, wherein the D/B converter comprises:

a splitter adapted to split the received data signal;

two comparators, each adapted to compare a copy of the received data signal to a specified threshold voltage; and

a logic gate adapted to generate the output signal from outputs from the two comparators.

26. The invention of claim 25, wherein:

the data signal is an NRZ binary data signal; and

the threshold voltages for the two comparators are selected such that one of the comparator outputs is always zero or always one.

27. The invention of claim 18, wherein:

the transmitter subsystem comprises a precoder adapted to precode a binary data signal, wherein the data signal transmitted through the electrical backplane is based on the precoded binary data signal;

the system comprises a filter adapted to filter the data signal prior to the data signal being interpreted as the duobinary data signal; and

the receiver subsystem comprises a duobinary-to-binary converter adapted to apply duobinary-to-binary conversion to the received data signal to generate a binary data signal.

28. The invention of claim 27, wherein:

the combination of the filter and the electrical backplane approximates a binary-to-duobinary converter; and

the duobinary-to-binary converter comprises:

a splitter adapted to split the received data signal;

two comparators, each adapted to compare a copy of the received data signal to a specified threshold voltage; and

a logic gate adapted to generate the output signal from outputs from the two comparators.

29. Apparatus for processing a data signal, comprising:

means for transmitting the data signal through an electrical backplane; and

means for receiving the data signal after being transmitted through the electrical backplane, wherein the received data signal is interpreted as a duobinary data signal.